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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,395	08/16/2001	Xiaowei Deng	TI-29319	4423
23494	7590	02/08/2005	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED P O BOX 655474, M/S 3999 DALLAS, TX 75265			LE, DON P	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 02/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/932,395

Applicant(s)

DENG, XIAOWEI

Examiner

Don P. Le

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 16 August 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 11-18 is/are allowed.
- 6) ☒ Claim(s) 1 and 6 is/are rejected.
- 7) ☒ Claim(s) 2-5, 7-10 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Esch, jr. (US 6,268,750).

3. With respect to claim 1, figure 1 of Esch disclose a circuit comprising:

a pull-up network (110) comprising a plurality parallel connected MOS transistors with a first (VDD) and second (102) common node, wherein least one said plurality parallel connected MOS transistors is a NMOS transistor (117) and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor (118);

a circuit supply voltage (VDD) which is connected to said first common node of said pull-up network;

a pull-down network (120) which is connected to said second common node of said pull-up network; and

an output node (102) which is connected to said second common node said pull-up network.

4. With respect to claim 6, figure 1 of Esch discloses a circuit comprising:

pull-down network (120) comprising a plurality of parallel connected MOS transistors with a first (GND) and second (148) common node, wherein at least one said plurality of parallel

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connected MOS transistors is a NMOS transistor (128) and at least one of said plurality of parallel connected MOS transistors is a PMOS transistor (127);

a circuit ground (GND) which is connected to said first common node said pull-down network;

a pull-up network (110) which is connected to said second common node of said pull-down network; and

an output node (PAD) which connected common node of said pull-down network.

***Allowable Subject Matter***

5. Claims 11-18 are allowed.

6. Claims 2-5 and 7-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is an examiner's statement of reasons for allowance:

With respect to claim 2, the prior art does not teach pull-down circuit having series connected MOS transistors.

With respect to claims 4 and 5, the prior art does not teach MOS transistors of a pull-up network has a gate tied to a floating substrate body.

With respect to claim 7, the prior art does not teach pull-up circuit having series connected MOS transistors.

With respect to claims 9 and 10, the prior art does not teach MOS transistors of a pull-down network has a gate tied to a floating substrate body.

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With respect to claim 11, the prior art does not teach a circuit having a pull-down network comprising a plurality of parallel connected PMOS transistors.

With respect to claim 15, the prior art does not teach a circuit having a pull-up network comprising a plurality of parallel connected NMOS transistors.

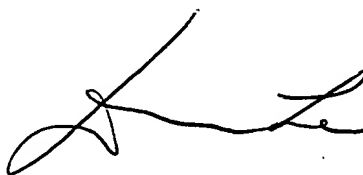
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

2/5/2005



**DON LE**  
**PRIMARY EXAMINER**